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Nonvolatile Memory Effect in Organic Thin-Film Transistor Based on Aluminum Nanoparticle Floating Gate

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A nonvolatile memory effect was observed in an organic thin-film transistor by introducing a floating gate structure. The floating gate was composed of an Al film in a thickness of nanometers, which was thermally deposited on a SiO2 insulator and exposed to air spontaneously oxidize. It can be seen that the transistors exhibit significant hysteresis behaviors and storage circles in current-voltage characteristics in the dark and under illumination, indicating that the transistors may act as a nonvolatile memory element. The operational mechanism is discussed in the cases of dark and illumination via charge trapping by the Al floating gate.

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In the past two decades, organic electronics have attracted considerable attention due to their flexibility, low cost and large area process for potential applications: flat-panel displays,[1] logical circuit,[2] solar cells,[3] sensors.[4] Recently, much attention is paid to organic memory devices[5–17] for applications like organic circuits in a radio-frequency identification tag or a smart card. One interesting option is to make a memory cell based on an organic thin-film transistor (OTFT) due to its non-destructive readout and single-transistor application.[18] Up to now, several methods have been used to fabricate OTFT memory devices. One way is to use ferroelectric materials, such as PbZrTiO3,[8] poly (vinylidenefluoridetri-fluoroethylene) (PVDF/TrFE),[9–13] nylon poly (m-xylylene adipamide) (MXD6),[14] or electret polyvinyl alcohol (PVA),[15] as the gate insulating layer. The direction of the polarization of the gate dielectric layer modulates the channel conductance, resulting in the memory characteristics of the OTFTs. Another way to make a TFT memory is by using a floating gate structure, where a floating gate is generally introduced into the gate dielectric. This approach has seen dramatic progresses in the field of silicon-based nonvolatile memory. However, the attempt of the floating gate TFT memory based on organic semiconductors is rarely reported.[16,17]

In this Letter, we report an OTFT-based memory device with the floating gate structure. The floated gate is formed by oxide a thin Al film in air. Clearly, a remarkable hysteresis loop can be observed in the drain-source current IDS via drain-source voltage VDS characteristics when sweeping the gate-source voltage VGS between +80 V to −80 V, and there exists a clear difference in the characteristics in dark and under illumination.

A heavily doped n-type silicon (n+–Si) with a 900 nm thermally growth SiO2 as the gate insulator was used as the substrate and gate. After routine cleaned, the substrates were put into the vacuum chamber. A 3-nm-thick Al film was first thermally evaporated onto the surface of SiO2 at a rate of about 0.6 Å/s under a pressure of 10−4 Pa. Next, the substrate was exposed to the cleaned dry air at room temperature for two minutes. Then the Al thin film was partially oxidized and finally many separated nanoparticle islands are formed, which could act as the floating gate. After exposed in air, the substrates were put in the vacuum chamber again. With the vacuum pressure of 10−4 Pa, a 30-nm-thick pentacene film was thermally deposited acting as the active layer at a rate of about 0.5 Å/s, and a 10 nm molybdenum oxidation (MoOx) and 100 nm Al as source-drain electrode were deposited by a shadow mask to finish the device. The utilization of MoOx may improve the injection of holes.[19] The result channel width W and length L are 2000 μm and 30 μm, respectively. During the deposition, the substrates were held at room temperature. A cross-section schematic diagram of the result devices is shown in the inset of Fig. 1(a). The electrical characteristics of the devices were measured using two Keithley 2400 source-measure units in the dark or
under illumination at room temperature within ambient air. The used light source is a fluorescent lamp with major spectral peaks in the 400–700 nm range and with an intensity of 1.8 mW/cm².

Figure 1(a) shows the output characteristic $I_{DS}$–$V_{DS}$ of a typical transistor in dark. The device features a p-channel field effect transistor. Furthermore, a clear hole accumulation mode and a slight hole depletion mode features can be observed, which means that some holes can accumulate in the channel at $V_{GS} = 0$ V. This hole depletion mode should be related to the memory effect of the transistor. When the device was illuminated by the fluorescent lamp, it is found that the operation current ($I_{DS}$, illumination) shows a large increase compared with that ($I_{DS}$, dark) in dark, and the feature of hole depletion mode becomes more notable (as shown in Fig. 1(b)). The inset in Fig. 1(b) shows the spectral response curve of the 30-nm-thick pentacene film.

Figures 2(a) and 2(b) show the transfer characteristic $I_{DS}$–$V_{GS}$ of the result transistor in dark and under illumination, respectively. It is clearly seen that significant hysteresis loops, in clockwise direction, are observed when cycling $V_{GS}$ is applied. Except for the first time sweeping, the hysteresis loops have a good repeatability. The memory ratio is defined as the ratio of $I_{DS}$ in different sweeping directions at the same $V_{GS}$. The largest values of memory ratio, 2.1 (in dark) and 11 (under illumination), can be obtained at $V_{GS} \approx 80$ V and +25 V, respectively, in the case of constant $V_{DS} = -10$ V. For the sweeping forward or backward, different threshold voltages $V_T$ can be extracted, which can be defined as the reading state “0” or “1”, respectively. The high negative ($-80$ V) or positive (80 V) $V_{GS}$ can be defined as the programming/erasing (P/E) voltage. The memory window voltages, defined as the difference of $V_{GS}$, as shown in the inset of Fig. 2(b). The ratio value reaches the maximum value of 102 at $V_{GS} = -3$ V in forward sweeping. The increase of $I_{DS}$ under illumination should be related to photo-induced hole accumulation at electric field.

Figure 3 shows typical storage cycles of present device at $V_{DS} = -10$ V in dark and illumination. The P/E voltages are chosen to be $V_{GS} = -80$ V and 80 V, respectively. The reading state of the memory
for 0/1 can also be carried out by monitoring $I_{DS}$ at $V_{GS} = -50 \text{ V}$ (in dark) or $V_{GS} = 0 \text{ V}$ (under illumination). High $I_{DS}$ denotes the 0 state of the memory unit and low $I_{DS}$ denotes the 1 state of the memory unit. It can be seen that the present OTFT shows better storage performance. The memory properties can be yet kept after 100 cycles. The data retention time of present transistor memory devices in dark and under illumination is illustrated in Fig. 4. The 0/1 state is obtained by P/E voltages of $-80 \text{ V}$ and $80 \text{ V}$ for 20s, respectively. In the measurement of $I_{DS}$ versus time, the reading voltage is fixed to be $-50 \text{ V}$ and $0 \text{ V}$ in dark and under illumination, respectively, with $V_{DS} = -10 \text{ V}$. The data retention time, with $I_0/I_1$ dropping to 50% of its initial value, is about 200s for the average result of dozen same devices, which can be compared with Ref. [16].

One possible explanation is the repeatable hysteresis and memory properties should be attributed to the utilization of the Al nanoparticle islands acting as the floating gate in dielectric. To demonstrate the role of Al nanoparticle islands, different thickness Al thin films are thermally grown as the floating gate. When the Al film is thicker than 3 nm, the hysteresis phenomenon of device transfer characteristics is more prominent, only with a slight decrease of $I_{DS}$. When the Al film is thinner than 2 nm (such as device B), the hysteresis is small, which indicates that the oxidation depth of the Al film is about 2 nm. For the reference structure transistors (device C) without any floating gate, only 900 nm SiO$_2$ acting as insulator, the hysteresis is near neglected. The transfer characteristics of devices B and C are shown in the inset of Fig. 2(a). The small hysteresis loops should be originated from the partial traps at inorganic/organic interface.

Actually, the Al nanoparticle islands as floating gate can act as the charge capture centre. The hysteresis processes can be well explained by energy level diagrams. Figure 5(a) shows the energy level diagrams of SiO$_2$/Al/Al$_2$O$_3$/pentacene without supplying $V_{GS}$, with supplying high negative $V_{GS}$ in dark (b), with supplying high positive $V_{GS}$ in dark, and with supplying high positive $V_{GS}$ under illumination (d).

![Fig. 4. Data retention of the present transistor memory device in dark (a) and under illumination (b).](image)

![Fig. 5. Energy level diagrams of SiO$_2$/Al/Al$_2$O$_3$/pentacene without supplying $V_{GS}$ (a), with supplying high negative $V_{GS}$ in dark (b), with supplying high positive $V_{GS}$ in dark, and with supplying high positive $V_{GS}$ under illumination (d).](image)
pentacene bends downward as indicated in Fig. 5(a). The schematic energy-band structure variations corresponding to P/E processes in dark and under illumination are shown in Figs. 5(b), 5(c) and 5(d). Here a qualitative explanation is given to illustrate the P/E processes. As we know, the pentacene is p-type semiconductor, and then no electron can accumulate in the channel in dark. In the case of dark, as \( \text{V}_{\text{GS}} \) sweeps in both directions, the hysteresis loops are in the negative \( \text{V}_{\text{GS}} \) region, demonstrating that only holes play role in the storage operation. Before \( \text{V}_{\text{GS}} \) is applied, the Al nanoparticle island floating gate should be neutral. When a large positive \( \text{V}_{\text{GS}} \) is initially applied, the holes in Al nanoparticle islands diffused from the channel can be ejected back. In this case, it needs a small negative \( \text{V}_{\text{GS}} \) to turn the transistor on, and then the first sweeping \( \text{I}_{\text{DS}}-\text{V}_{\text{GS}} \) curve in forward (e.g. \( \text{V}_{\text{GS}} \) swept from 80 V to \(-80 \text{ V}\)) locates in left. When a large negative \( \text{V}_{\text{GS}} \) is applied, the energy band of pentacene greatly bends upward, the holes may be injected to the Al nanoparticles floating gate from the channel by direct tunneling process and captured in the Al nanoparticle islands, as shown in Fig. 5(b), then the programming is performed. The captured holes generate an internal electric field \( E_i \) along the direction opposite to the applied \( \text{V}_{\text{GS}} \) and this \( E_i \) weakens the external applied electric field \( E_{oe} \) effects. Thus the \( \text{I}_{\text{DS}} \) swept backward is smaller than swept forward at the same \( \text{V}_{\text{GS}} \), and a more negative \( \text{V}_{\text{GS}} \) is needed to turn the device on; that is, a right shift of \( V_T \) occurs. When a high positive \( \text{V}_{\text{GS}} \) is applied again, that is, the 2nd \( \text{I}_{\text{DS}}-\text{V}_{\text{GS}} \) curve forward sweeping, the orbital energy level bends downward and the holes stored in the Al nanoparticles have chances to be ejected back into the pentacene channel by tunneling, as shown in Fig. 5(c). The erasing process is performed. However, there exists an additional FN tunnelling for holes through the space charge region at the pentacene surface near to \( \text{Al}_2\text{O}_3 \). As a result, the holes stored in the floating gate will be partly ejected into the channel, and others will remain in the floating gate. Affected by the \( E_i \) induced by these remained holes, the 2nd \( \text{I}_{\text{DS}}-\text{V}_{\text{GS}} \) curve swept forward shifts to left although it cannot return to the initial position. When the \( \text{V}_{\text{GS}} \) sweeps backward again, the \( \text{I}_{\text{DS}}-\text{V}_{\text{GS}} \) curve shifts to right. Thus a P/E cycle is performed as memory in dark. When illuminated, the electron-hole pairs generate in the channel. At a positive supplied \( \text{V}_{\text{GS}} \), the orbital energy level bends downwards, as shown in Fig. 5(d). The photo-induced electrons have chances of being injected from the channel into the floating gate through the direct tunneling process. After combined with the remained holes, the redundant electrons are captured in the Al nanoparticles, and an \( E_i \) is generated, further weakening the external applied electric field effects. Taking into account the photo-induced holes, the transistor can turn on at a positive \( \text{V}_{\text{GS}} \). Similarly, when a large negative \( \text{V}_{\text{GS}} \) is supplied, the stored electron have chances of being ejected from the floating gate into the channel through the FN tunneling process, and more holes are injected into the floating gate through the direct tunneling process. After combined with the stored electron, the redundant holes are captured in the Al nanoparticles, thus generating an \( E_i \), also weakening the external applied electric field effects. Taking into account the photo-induced holes, the \( \text{I}_{\text{DS}}-\text{V}_{\text{GS}} \) curve shifts right remarkably, but be more left than that in dark. Thus a P/E cycle is performed under illumination.

In conclusion, a nonvolatile organic thin-film transistor memory has been demonstrated by introducing Al nanoparticles as a floating gate. The significant hysteresis behaviors and storage circles can be obtained in the dark and under illumination, respectively. It is hopeful that the memory ratio and the data retention time can be improved by optimizing the floating gate Al nanoparticle density and the interface of alumina/pentacene.

References